

077653017

IR-1013(Cont) (2-563)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of  
Alexander Lidow et al  
Serial No.:  
Filed:  
For: PLURAL POLYGON SOURCE P.

New York, New York  
Date: February 8, 1991  
Group Art Unit:  
Examiner:

Hon. Commissioner of Patents and Trademarks  
Washington, D.C. 20231

PRELIMINARY AMENDMENT

**Sir:**

Preliminary to the examination of the above application, please amend this application as follows:

IN THE SPECIFICATION:

Page 1, line ~~2~~, delete "copending";

lines 3 and 4, delete "951,310 (IR-664),

filed October 13, 1978" and insert

therefor  $\approx$  951,310, filed October

13, 1978, now abandoned and

refiled as continuation applica-

tion Serial No. 232,713, filed

February 9, 1981, now U.S. Patent

4,376,286 A;

line 12, ~~delete~~ "copending application"

Serial No. 951,310" and insert

therefor -- U.S. Patent

4,376,286 --;

lines 19 and 20, delete "copending applica-  
tion Serial No. 951,310" and

insert therefor -- U.S. Patent  
4,376,286 --;

Page 2, line 11, delete "application Serial No.  
951,310" and insert therefor --  
U.S. Patent 4,376,286 --;  
lines 17 and 18, delete ", however,".

Page 4, line 12, delete "copending application  
Serial No. 951,310" and insert  
therefor -- U.S. Patent 4,376,286,  
referred to above --;

Page 5, line 21, change "distance" to -- depth --;  
*Loke* *NE* line 12, after "drain 51." please insert --  
*2/11/92*  
*W.E.* Note that channels labeled 60 and  
61 of Figure 5 are the same  
annular channel which is formed  
within the region 22. Similarly,  
channels 62 and 63 are the same  
annular channel formed in the  
region 23. --

lines 34 and 35, delete "above noted  
copending application Serial No.  
951,310" and insert therefor --  
U.S. Patent 4,376,286, referred to  
above, --;

Page 7, line 3, delete "the" (first occurrence);  
line 23, change "55" to -- 50 --;

Page 8, line 24, after "P+" insert -- (shown as "P"  
in the drawings) --.

IN THE DRAWINGS:

Please amend Figs. 1, 3, 4 and 5 as shown in red on  
the attached copy thereof.

W  
P  
N  
K  
CM  
IN THE CLAIMS:

Please cancel claim 1.

Please add the following new claims:

12. A high power MOSFET device having more than  
B1000 parallel-connected individual FET devices closely packed  
into a relatively small area comprising;

5 P1 a thin wafer of semiconductor material having first  
and second spaced, parallel planar surfaces; at least a first  
portion of the thickness of said wafer which extends from said  
first planar surface consisting of an epitaxially deposited  
region of a first conductivity type;

P1 a plurality of symmetrically disposed laterally  
distributed hexagonal base regions each having a second con-  
ductivity type formed in said epitaxially deposited region and  
extending for a given depth beneath said first planar surface;

P1 said hexagonal base regions spaced at said first  
surface from surrounding ones by a symmetric hexagonal lattice  
of semiconductor material of said first conductivity type;

P1 each side of each of said hexagonal base regions  
being parallel to an adjacent side of another of said hexago-  
nal base regions;

P1 a hexagonal annular source region of said first  
conductivity type formed in an outer peripheral region of each  
of said hexagonal base regions and extending downwardly from  
said first planar surface to a depth less than the depth of  
said base regions;

25 P1 an outer rim of each of said annular source regions  
being radially inwardly spaced from an outer periphery of its  
respective hexagonal base region to form an annular channel  
between each of said outer rims of said annular source regions  
and said symmetric hexagonal lattice of semiconductor material  
of said first portion of said wafer;

30 P1 a common source electrode formed on said first

planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;

35 *p/* a drain electrode connected to said second planar surface of said wafer;

*p/* an insulation layer means on said first planar surface and overlying at least said annular channels;

*p/* a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels; and

40 *p/* a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

*2*  
13. The device of claim *12* wherein said annular channels have at least one leg in longitudinal alignment with other legs of other of said annular channels; said plurality of spaced locations disposed along a line defined by said legs of said annular channels which are in longitudinal alignment.

*3*  
14. A high power MOSFET device having more than *B* 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

5 *p/* a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

*B* 10 *p/* a plurality of symmetrically disposed laterally distributed polygonal base regions each having a second conductivity type formed in said *epitaxially deposited* ~~lightly doped~~ region and extending for given depth beneath said first planar semiconductor surface;

15 *p1* said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

*p1* each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;

20 *p1* a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

25 *p1* an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;

*p1* a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;

35 *p1* a drain electrode connected to said second planar semiconductor surface of said wafer;

*p1* an insulation layer means on said first planar surface and overlying at least said annular channels;

40 *p1* a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels; and

*p1* a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations  
45 over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

4  
15. The device of claim 14 wherein said annular channels have at least one leg in longitudinal alignment with other legs of other of said annular channels; said plurality of spaced locations disposed along a line defined by said legs of said annular channels which are in longitudinal alignment.

5  
16. A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising;

PI a wafer of semiconductor material having planar first and second opposing semiconductor surface; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

PI a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type; the space between adjacent ones of said polygonal base regions defining a common conduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;

PI a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

<sup>P1</sup> a common source electrode means connected to said polygonal annular source regions and their respective base regions;

35 <sup>P1</sup> gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

<sup>P1</sup> gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

40 <sup>P1</sup> a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

<sup>P1</sup> a drain electrode coupled to said drain conductive region; and

<sup>P1</sup> a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

5 <sup>6</sup> 17. The device of claim <sup>5</sup> 16 wherein said annular channels have at least one leg in longitudinal alignment with other legs of other of said annular channels; said plurality of spaced locations disposed along a line defined by said legs of said annular channels which are in longitudinal alignment.

<sup>7</sup> 18. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

5 <sup>P1</sup> a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

10 p1 at least first and second spaced base regions of a  
second conductivity type formed in said wafer and extending  
downwardly from said first planar semiconductor surface to a  
first depth beneath said first planar semiconductor surface;  
the space between said at least first and second spaced base  
regions defining a common conduction region of a first conduc-  
15 tivity type at a given first planar semiconductor surface  
location; said common conduction region extending downwardly  
from said first planar semiconductor surface;

20 p1 first and second annular source regions of said  
first conductivity type formed in said first and second spaced  
base regions respectively at said first planar semiconductor  
surface locations to a depth less than said first depth; said  
first and second annular source regions being laterally spaced  
along said first planar semiconductor surface from the facing  
respective edges of said common conduction region thereby to  
25 define first and second channel regions along said first  
planar semiconductor surface between each pair of said first  
and second annular source regions, respectively, and said  
common conduction region; each of said first and second chan-  
nel regions being coplanar with one another;

30 p1 a common source electrode means connected to said  
first and second annular source regions and their respective  
first and second base regions;

35 p1 gate insulation layer means on said first planar  
semiconductor surface, disposed at least on said first and  
second channel regions;

p1 gate electrode means on said gate insulation layer  
means and overlying said first and second channel regions;

40 p1 a drain conductive region remote from said common  
conduction region and separated therefrom by said relatively  
lightly doped major body portion and extending to said second  
semiconductor surface;

p1 a drain electrode coupled to said drain conductive  
region;



45 P1 each of said at least first and second spaced base  
regions having a polygonal configuration; each of said first  
and second annular source regions having a polygonal configu-  
ration conforming to that of their respective base region; and  
P1 a gate pad electrode section on the surface of said  
device and at least one finger extending from said gate pad;  
50 said at least one finger electrically contacting said  
polysilicon gate electrode at a plurality of spaced locations  
over the surface of said polysilicon gate electrode, thereby  
to reduce the R-C delay constant of said device.

19. The device of claim 18 wherein said annular  
channels have at least one leg in longitudinal alignment with  
other legs of other of said annular channels; said plurality  
of spaced locations disposed along a line defined by said legs  
of said annular channels which are in longitudinal  
alignment. A

END

REMARKS

The present application is a continuation of  
copending parent application Serial No. 07/291,423, filed  
December 23, 1988.

This application now contains claims 12-19. An  
early examination of the claims is requested.

EXPRESS MAIL CERTIFICATE

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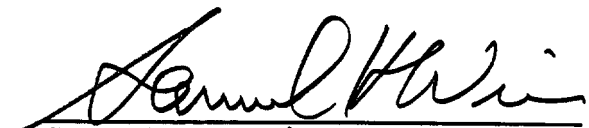
Signature

February 8, 1991

Date of Signature

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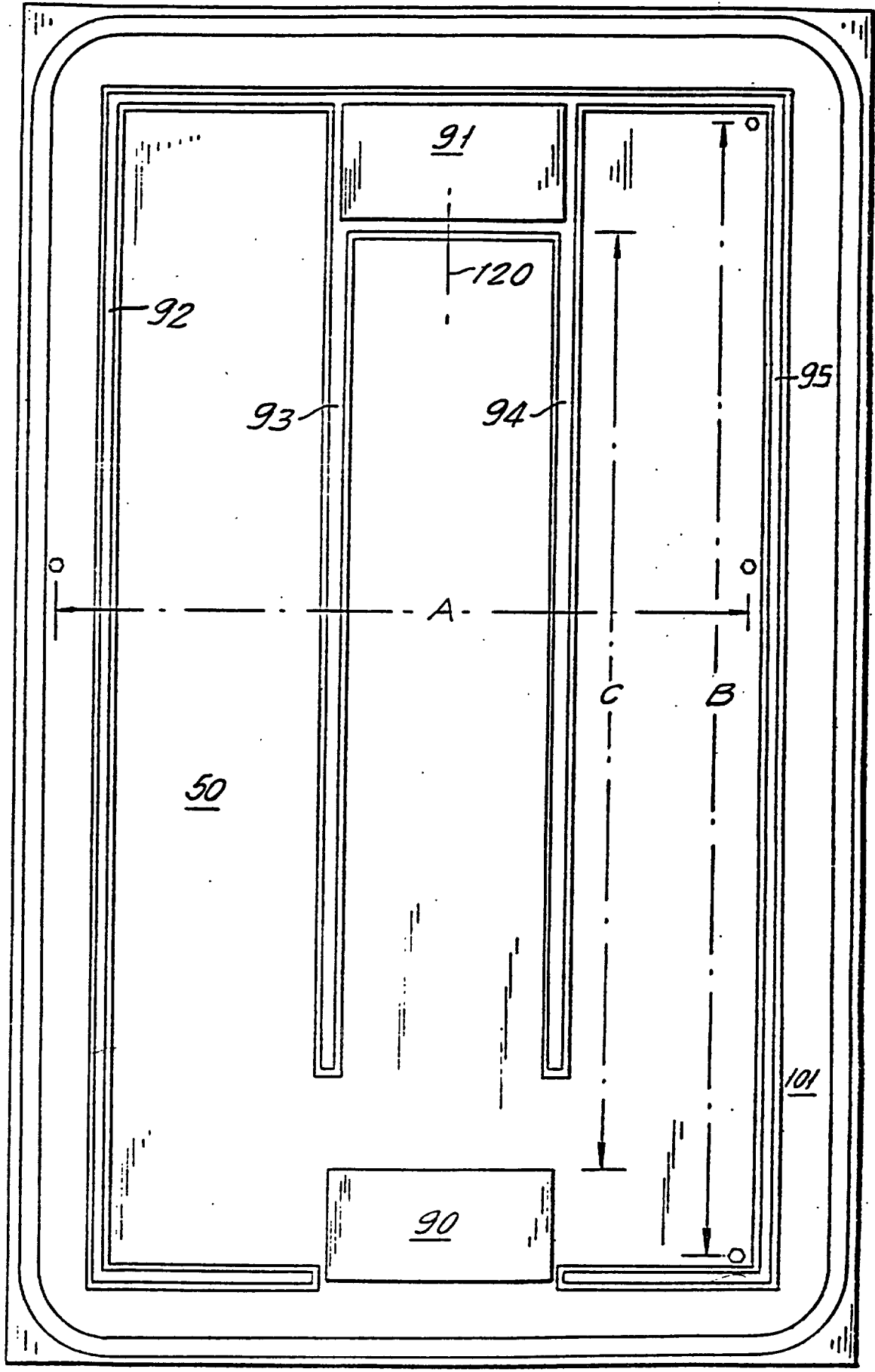
Respectfully submitted,



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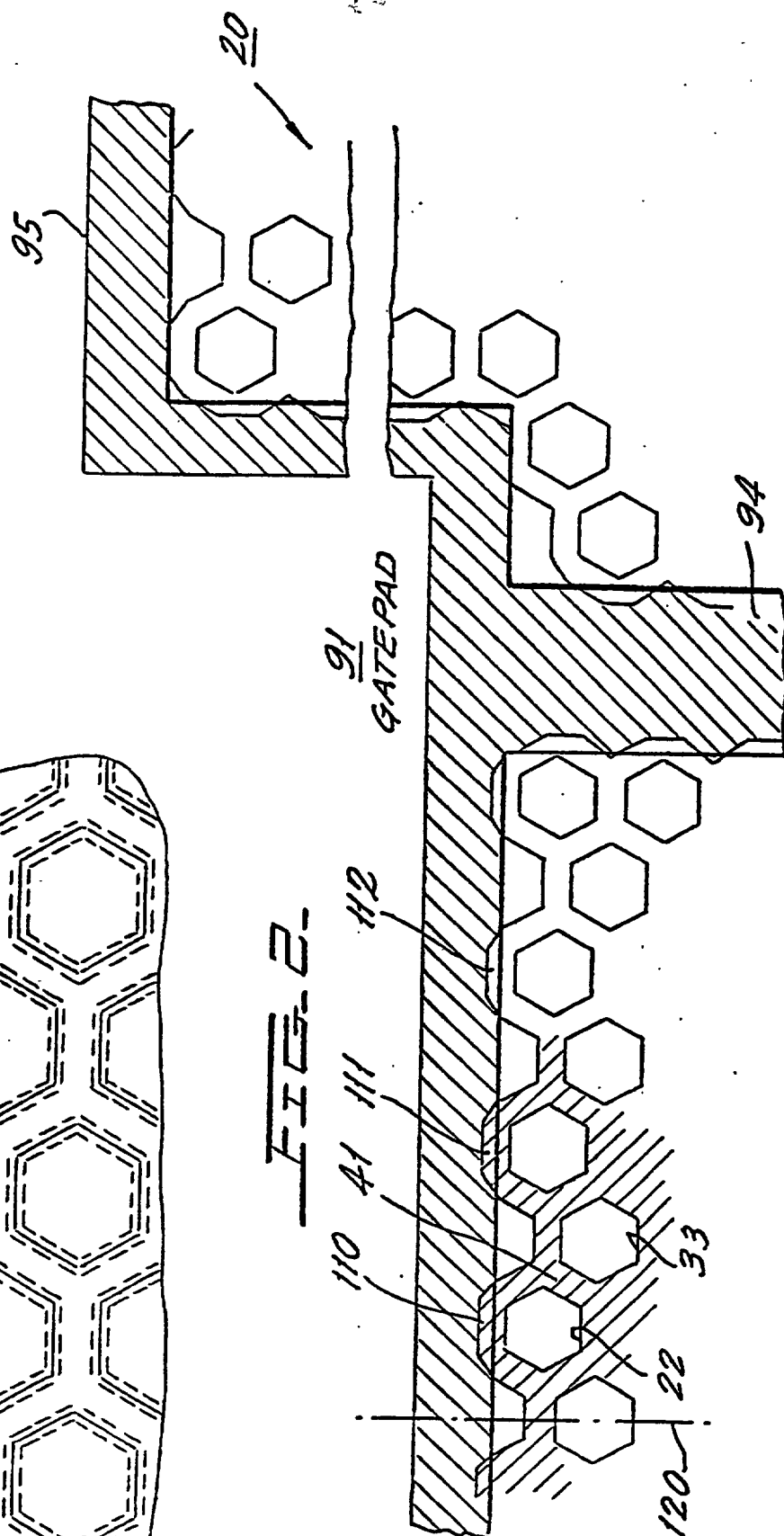
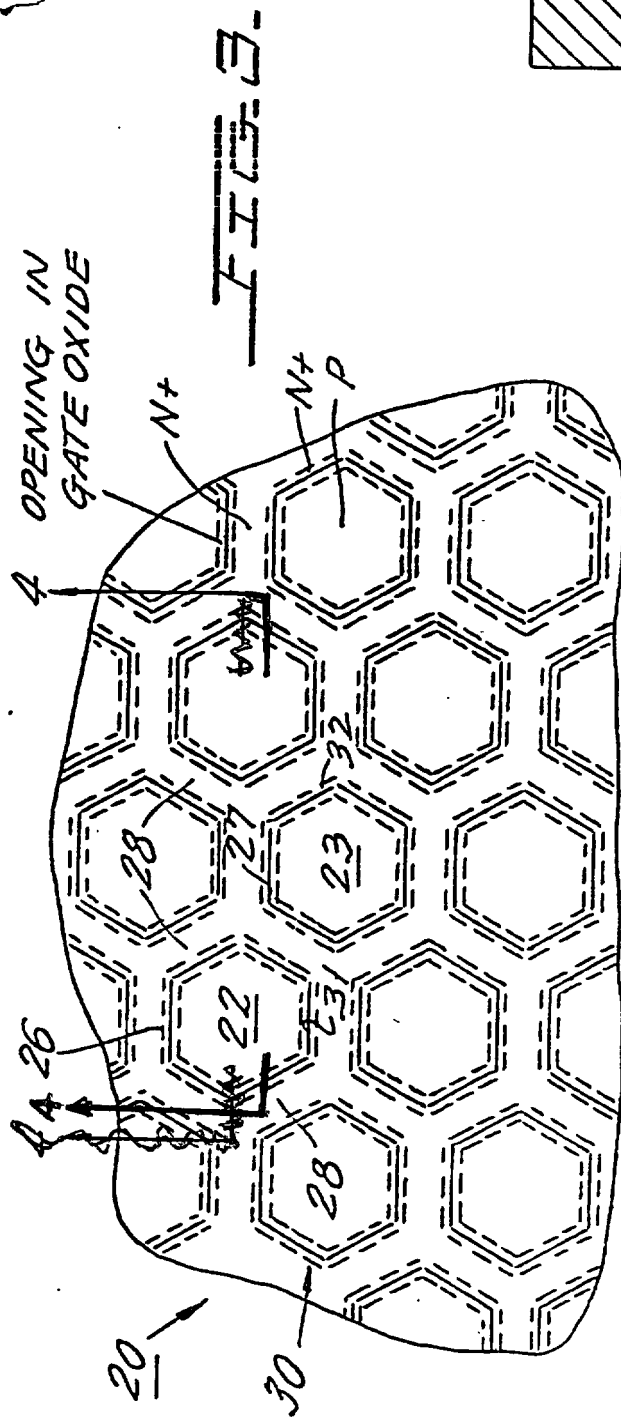


FIG. 4

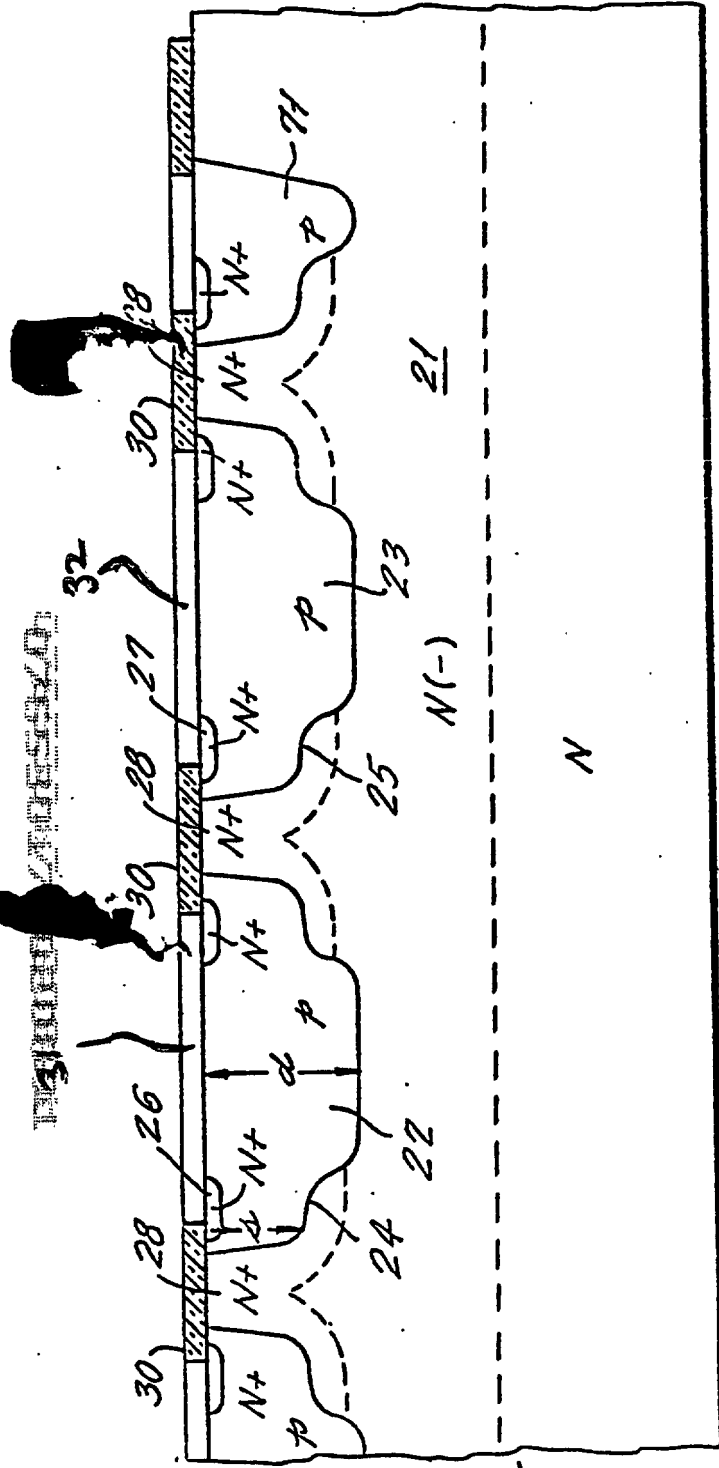


FIG. 5

